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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/371,955	08/11/99	LEIPHART	M4065.0196/P

EXAMINER	
ART UNIT	PAPER NUMBER

MM91/0102

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WASHINGTON DC 20037-1526

DATE MAILED: 01/02/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

04/02/04

Office Action Summary	Application No.	Applicant(s)	
	09/371,955	LEIPHART, SHANE P.	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-40 is/are pending in the application.

4a) Of the above claim(s) 1-25 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 26-40 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II (claims 26-40) in Paper No. 4 is acknowledged.

Drawings

2. The drawings in this application are objected to by the Draftsperson as informal. Any drawing corrections requested, but not made in the prior application should be repeated in this application if such changes are still desired. If the drawings were changed and approved during the prosecution of the prior application, a petition may be filed under 37 CFR 1.182 requesting the transfer of such drawings, provided the parent application has been abandoned. However, a copy of the drawings as originally filed must be included in the 37 CFR 1.60 application papers to indicate the original content.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 26-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Harada et al (US 5,313,101).

Regarding claim **26**, Harada et al discloses a semiconductor device comprising (Fig. 2G):

a metallic layer (4) over a substrate; a dielectric layer (5) on the metallic layer; a via hole extending through the dielectric layer to a surface of the metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; and a conductive material (103') formed on the titanium aluminide liner.

Regarding claim **27**, Harada et al discloses a semiconductor device comprising (Fig. 2G):

an aluminum layer (4) over a substrate; a dielectric layer (5) on the aluminum layer; a via hole extending through the dielectric layer to a surface of the aluminum layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium nitride layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium nitride layer; and a metallic layer (103)on the dielectric layer and electrically connected to the plug material.

Regarding claim **28**, Harada et al discloses a semiconductor memory device, comprising (Fig. 2G):

a memory circuit region in a semiconductor substrate; a first dielectric layer (3) over the memory circuit region; a first metallic layer (4) over the first dielectric layer; a contact interconnect between the first metallic layer (4) and the substrate (1); a second dielectric layer (5) on the first metallic (aluminum) layer; a via hole extending through the second dielectric layer to a surface of the second metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium compound layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium

compound layer; and a second metallic layer (103) on the second dielectric layer and electrically connected to the plug material.

Regarding claim **29**, Harada et al discloses the titanium compound layer (102) being titanium nitride. See Col.10, line 25.

Regarding claim **30**, Harada et al discloses the first metallic layer (4) comprising aluminum. See Col.10, line 42.

Regarding claim **31**,

Regarding claim **32**, Harada et al discloses the memory circuit including a DRAM cell (2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims **33-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al (US 5,313,101) in view of Clayton (US 4,656,605).

Regarding claim **33**, Harada et al discloses a semiconductor device comprising (Fig. 2G):

a first metallic layer (4) over a substrate; a dielectric layer (5) on the first metallic layer; a via hole extending through the dielectric layer to a surface of the first metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium compound layer (102) formed on the titanium aluminide layer; a conductive material

(103') formed on the titanium compound layer; and a second metallic layer on the dielectric and electrically connected to the plug material.

Harada et al does not teach a memory module which include a semiconductor device as teaching by himself.

However, Clayton teaches the memory module comprising (Fig.2):

a substrate comprising a circuit board (31); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprises a random access memory (RAM) fabricated on a semiconductor substrate; and an edge connector (20) along one edge of the substrate in which is wired to said memory circuit. Clayton does not teach what semiconductor substrate (device) comprising. It would have been obvious to one of ordinary skill in the at the time the invention was made to have module system in order to complete the semiconductor memory device.

Regarding claim **34**, Harada et al discloses a semiconductor device comprising (Fig. 2G):

a metallic layer (4) over a substrate; a dielectric layer (5) on the metallic layer; a via hole extending through the dielectric layer to a surface of the metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a conductive material (103') formed on the titanium aluminide layer; and a second metallic layer on the dielectric and electrically connected to the plug material.

Harada et al does not teach a memory module which include a semiconductor device as teaching by himself.

However, Clayton teaches the memory module comprising (Fig.2):

a substrate comprising a circuit board (31); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprises a random access memory (RAM) fabricated on a semiconductor substrate which comprising the teaching of Harada; and an edge connector (20) along one edge of the substrate which is wired to said memory circuit.

It would have been obvious to one of ordinary skill in the at the time the invention was made to have module system in order to complete the semiconductor memory device.

Regarding claim **35**, Harada et al discloses a semiconductor device comprising (Fig. 2G):

an aluminum layer (4) over a substrate; a dielectric layer (5) on the aluminum layer; a via hole extending through the dielectric layer to a surface of the aluminum layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium nitride layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium nitride layer; and a metallic layer (103)on the dielectric layer and electrically connected to the plug material.

Harada et al does not teach a memory module which include a semiconductor device as teaching by himself.

However, Clayton teaches the memory module comprising (Fig.2):

a substrate comprising a circuit board (31); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more

of the memory chips comprises a random access memory (RAM) fabricated on a semiconductor substrate which comprising the teaching of Harada; and an edge connector (20) along one edge of the substrate which is wired to said memory circuit.

It would have been obvious to one of ordinary skill in the at the time the invention was made to have module system in order to complete the semiconductor memory device.

Regarding claim **36**, Harada et al discloses a semiconductor memory device, comprising (Fig. 2G):

a memory circuit region in a semiconductor substrate; a first dielectric layer (3) over the memory circuit region; a first metallic layer (4) over the first dielectric layer; a contact interconnect between the first metallic layer (4) and the substrate (1); a second dielectric layer (5) on the first metallic (aluminum) layer; a via hole extending through the second dielectric layer to a surface of the second metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium compound layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium compound layer; and a second metallic layer (103) on the second dielectric layer and electrically connected to the plug material.

Harada et al does not teach a memory module which include a semiconductor device as teaching by himself.

However, Clayton teaches the memory module comprising (Fig.2):

a substrate comprising a circuit board (31); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more

of the memory chips comprises a random access memory (RAM) fabricated on a semiconductor substrate which comprising the teaching of Harada; and an edge connector (20) along one edge of the substrate which is wired to said memory circuit.

It would have been obvious to one of ordinary skill in the at the time the invention was made to have module system in order to complete the semiconductor memory device.

7. Claims **37-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al (US 5,313,101).

Regarding claim **37**, Harada et al discloses a semiconductor memory device, comprising (Fig. 2G):

a first metallic layer over a substrate; a dielectric layer (3) over the first metallic layer (4); a via hole extending through the second dielectric layer to a surface of the second metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium compound layer (102) formed on the titanium aluminide layer; a conductive material (103') formed on the titanium compound layer; and a second metallic layer (103) on the dielectric layer and electrically connected to the plug material.

Harada et al does not teach a computer system in which comprises a semiconductor device as teaching by Harada et al. It would have been obvious to one of ordinary skill in the art to have a processor in computer system since a RAM fabricated on a semiconductor chip communicates with the processor while computer is operating.

Regarding claim **38**, Harada et al discloses a semiconductor memory device, comprising (Fig. 2G):

a metallic layer (4) over a substrate; a dielectric layer (5) on the metallic layer; a via hole extending through the dielectric layer to a surface of the metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; and a conductive material (103') formed on the titanium aluminide liner.

Harada et al does not teach a computer system in which comprises a semiconductor device as teaching by Harada et al. It would have been obvious to one of ordinary skill in the art to have a processor in computer system since a RAM fabricated on a semiconductor chip communicates with the processor while computer is operating.

Regarding claim **39**, Harada et al discloses the semiconductor device comprising (Fig.2G);

Harada et al discloses a semiconductor device comprising (Fig. 2G):

an aluminum layer (4) over a substrate; a dielectric layer (5) on the aluminum layer; a via hole extending through the dielectric layer to a surface of the aluminum layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium nitride layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium nitride layer; and a metallic layer (103)on the dielectric layer and electrically connected to the plug material.

Harada et al does not teach a computer system in which comprises a semiconductor device as teaching by Harada et al. It would have been obvious to one of

ordinary skill in the art to have a processor in computer system since a RAM fabricated on a semiconductor chip communicates with the processor while computer is operating.

Regarding claim **40**, Harada et al discloses a semiconductor memory device, comprising (Fig. 2G):

a memory circuit region in a semiconductor substrate; a first dielectric layer (3) over the memory circuit region; a first metallic layer (4) over the first dielectric layer; a contact interconnect between the first metallic layer (4) and the substrate (1); a second dielectric layer (5) on the first metallic (aluminum) layer; a via hole extending through the second dielectric layer to a surface of the second metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium compound layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium compound layer; and a second metallic layer (103) on the second dielectric layer and electrically connected to the plug material.

Harada et al does not teach a computer system in which comprises a semiconductor device as teaching by Harada et al. It would have been obvious to one of ordinary skill in the art to have a processor in computer system since a RAM fabricated on a semiconductor chip communicates with the processor while computer is operating.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Donghee Kang** whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DHK
December 22, 2000

Steven Loke
Primary Examiner